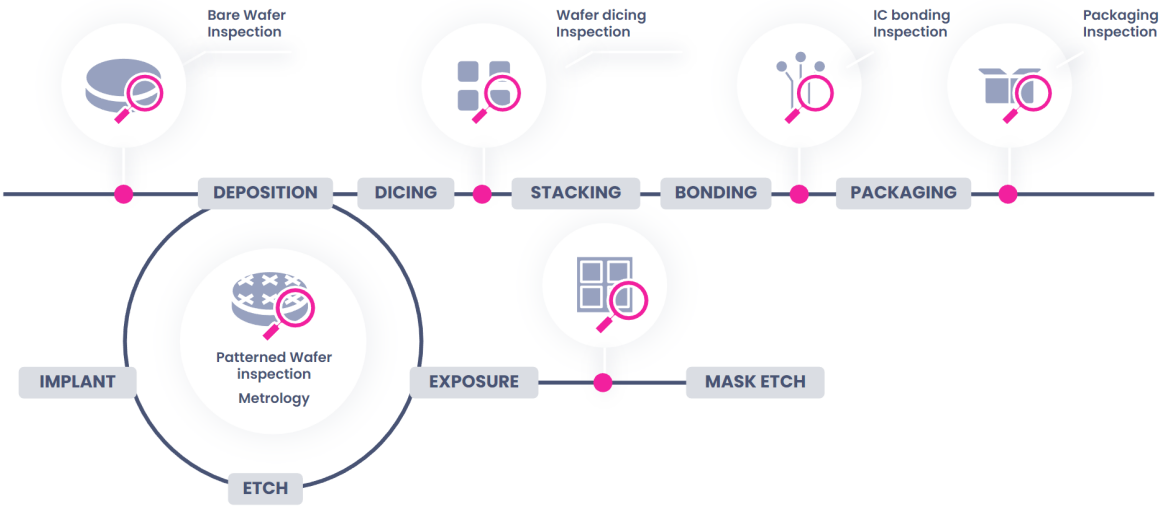
AI-BASED DEFECT CLASSIFICATION IN THE SEMICONDUCTOR INDUSTRY: AN ACCURACY AND EFFICIENCY BOOST

1. Introduction

Production yield is regarded as the single-most important factor in controlling wafer processing costs. It affects output per unit of input resources, waste generation, time to market and costs. Hence, yield improvements can provide significant competitive advantages, which are critical in unpredictable economic environments and help reaching sustainability goals of the semiconductor industry.

Semiconductor manufacturers can minimise defects and improve their overall yield by implementing rigorous inspections. Rigorous inspections involve a variety of quality control measures, including visual inspections designed to catch any defects or abnormalities in the manufacturing process and to ensure that every product meets the strict quality standards set by the end user industry.



What are the challenges?

Yield issues in the semiconductor industry primarily occur due to the highly complex manufacturing processes. The need to implant more transistors on a given chip year after year requires continuous improvement in sensitivity of inspection equipment. On top of the sensitivity requirement, there are factors like coverage, speed and throughput.

The growing complexity of Integrated Circuit (IC) architectures poses a challenge for accurate imaging and detection of defects. As IC structures become more three-dimensional and incorporate new materials, achieving complete and precise imaging becomes more difficult. It is not only crucial to identify defects but also to characterise them accurately.

Furthermore, the shift towards high-mix low-volume production schemes presents challenges for cost-effective automated inspections. The development, introduction, and operation costs need to be justified in the context of changing production patterns.

The automotive segment, in particular, imposes higher demands on defect inspection. It requires a higher sampling rate for inspection and employs stricter screening criteria. Automotive applications often involve safety-critical components, making the need for higher-quality chips even more crucial.

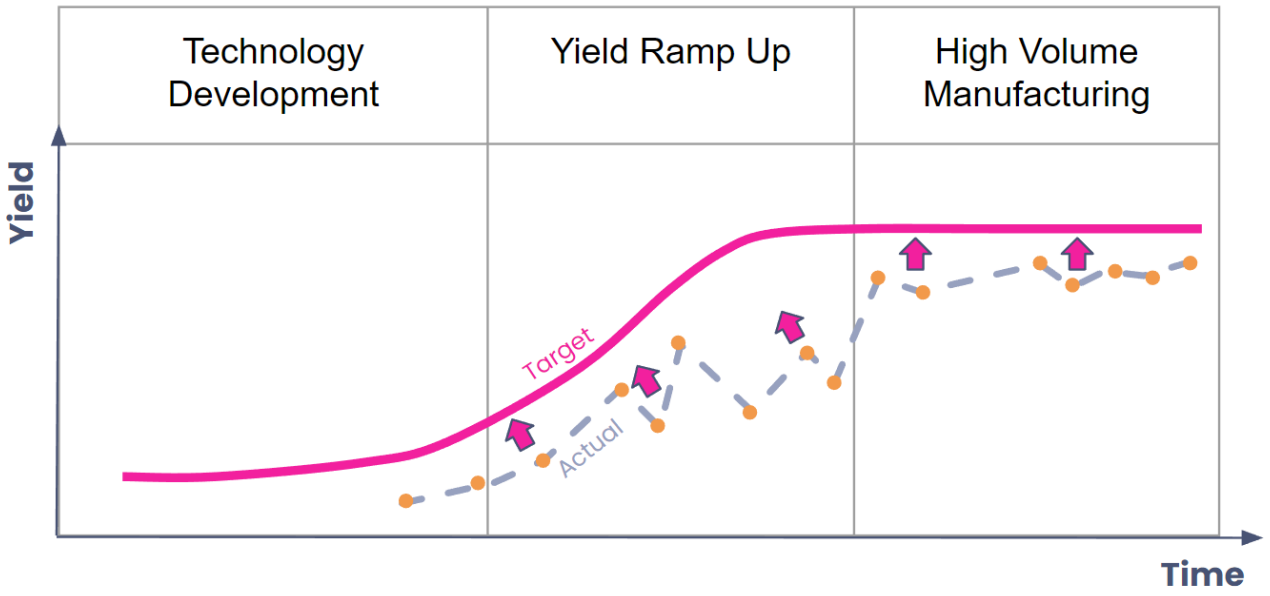
In summary, the semiconductor industry is driven by a universal push for higher-quality chips across various device types and design nodes. To achieve this, continuous improvements in inspection solutions, addressing the challenges of complex IC architectures, and adapting to changing production patterns are essential.

The importance of wafer inspection

Semiconductor wafer production sites use inspection systems, which typically include tools for optical wafer inspection and scanning electron microscope (SEM)-based review, for process monitoring. While both SEMs and optical inspection systems are used for defect detection in semiconductor wafer production, they differ in the type of defects they can detect and the resolution of their imaging capabilities.

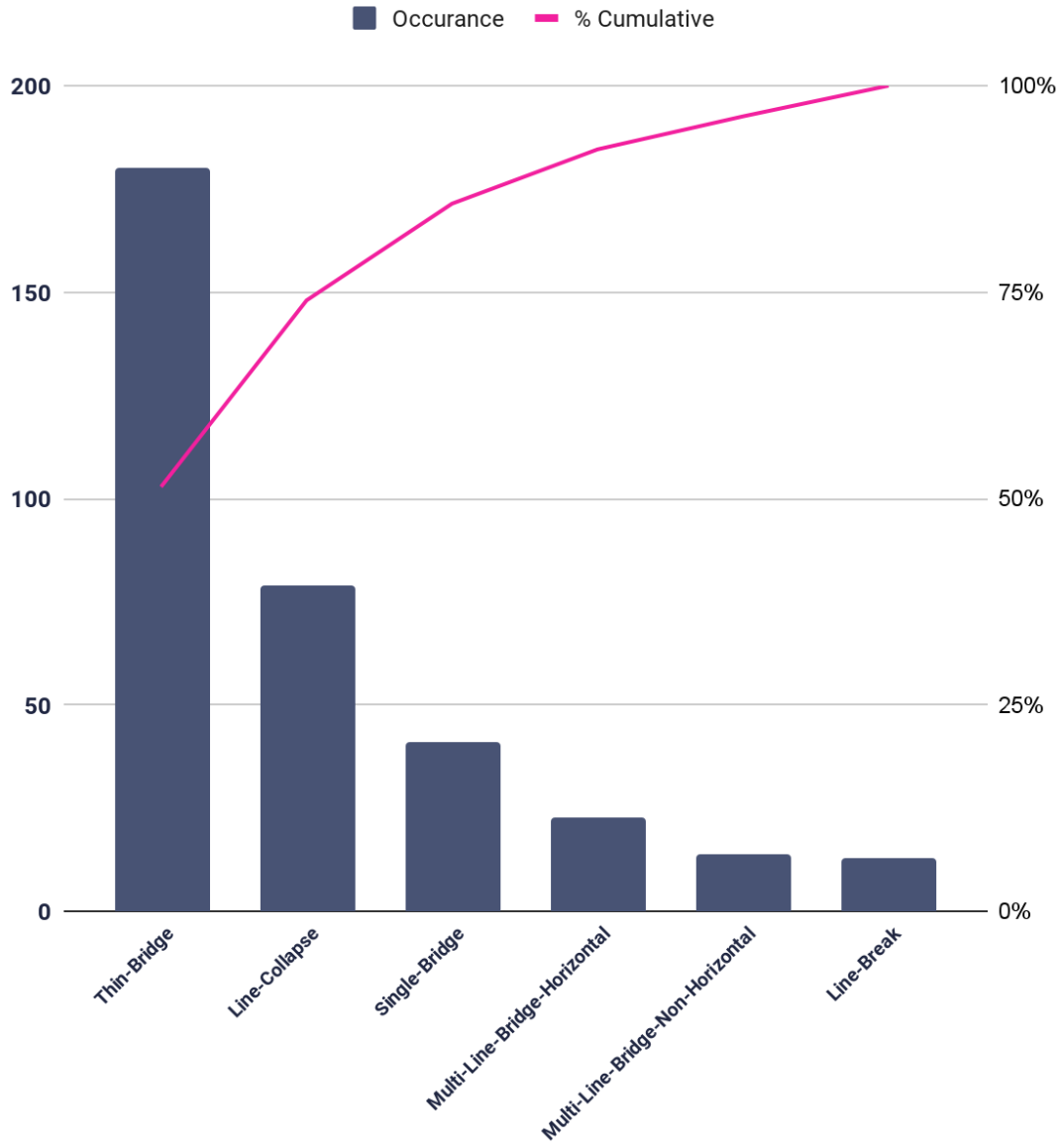
Many production sites use a combination of both imaging tools where an optical microscope is used to detect gross defects and SEMs can observe those defects in more detail while observing micro-defects that are not visible using optical microscopy. To design fabrication recipes and maintain process window parameters, chipmakers depend on wafer inspection, defect classification and review, metrology, and statistical analysis.

Throughout the various stages of semiconductor production - from initial process technology development to yield ramp up and high volume manufacturing for a new node - the most crucial support functions for improving and maintaining yield are: in-line wafer inspection technology in general, and wafer defect classification more specifically. The characterisation of defects allows chip manufacturers to identify the root cause of problems and take appropriate corrective action for faster ramp up and time-to-market.



2. Defect classification as enabler for yield ramp up and comprehensive process control

Defect classification is the act of allocating an image of a certain defect to a defect category. The goal of the classification is to decrease the number of defects that go unnoticed and to be able to predict maintenance needs in advance. It is important to have a highly accurate list of yield-limiting defects sorted by category, which is known as a fully-classified Pareto. This list helps engineers to quickly identify the specific types of defects causing the issue and get to the root of the problem more efficiently.



Performing manual classification of defects is labour intensive, repetitive and requires highly trained employees. On top of that, results can vary from operator to operator. This makes that the end result for manual classification is often a lower accuracy compared to automated classification. Also, defects cannot be classified by people at scale due to limitations of the human eyes and brains.

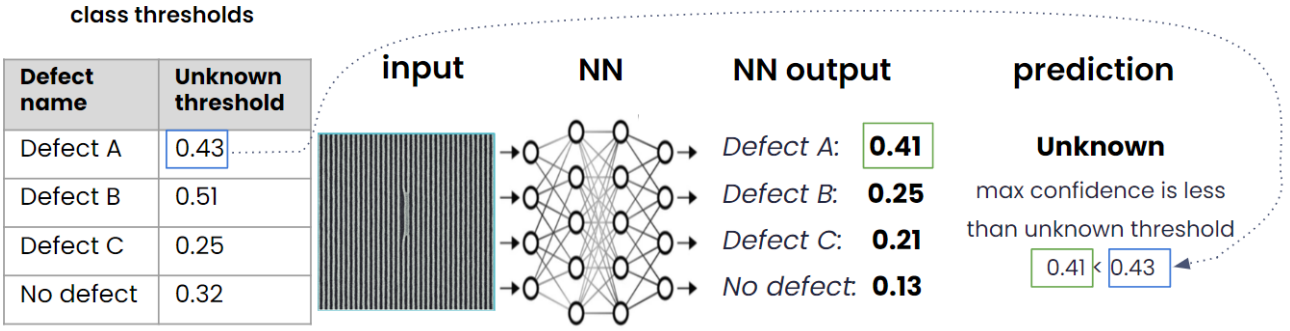
Although the introduction of Automatic Defect Classification (ADC) solutions mitigates the heavy load on human resources in fabrication, there remains an application mismatch between low classification accuracy and the high purity needs. Deep Learning AI-based classifiers increase accuracy (intelligence) in defect classification for both existing and newly-found defect types from an assortment of wafer designs.

Defect Classification	Manual	Automatic	AI based
Speed	✓	✓	✓
Accuracy	✓	✗	✓
Consistency	✗	✓	✓
Operator Training	✗	✓	✓
Product Mix Agility	✓	✗	✓

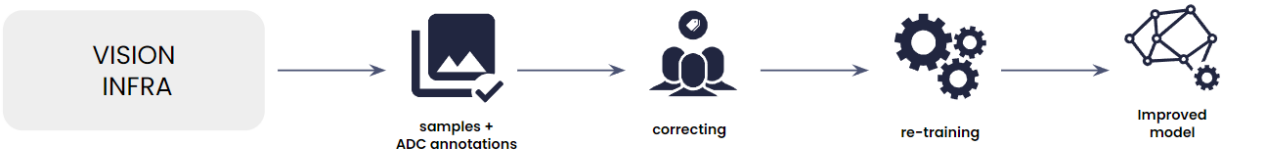
3. AI-based Automatic Defect Classification to the rescue

Progressively improving accuracy

Technically, a Deep Learning AI model produces a set of confidence values for each class and then selects the class with the highest confidence score as its prediction. During semiconductor manufacturing, classifications that do not meet the required confidence level (class threshold) for a specific class will be labelled as "Unknown" and are presented to the operator for manual classification.



The manual classification augments the existing labelled data and is then used to retrain the Machine Learning model. This way of working avoids the time consuming process of collecting new data for the unseen defects.



A dataset is collected together with the predictions of inference and stored on the storage server

A dataset with predictions is imported into Robovision AI by the operator/supervisor

Predictions/annotations are corrected by operator/supervisor

The base model is selected for transfer learning. Training data is split and training settings are selected

An improved version of the model is created

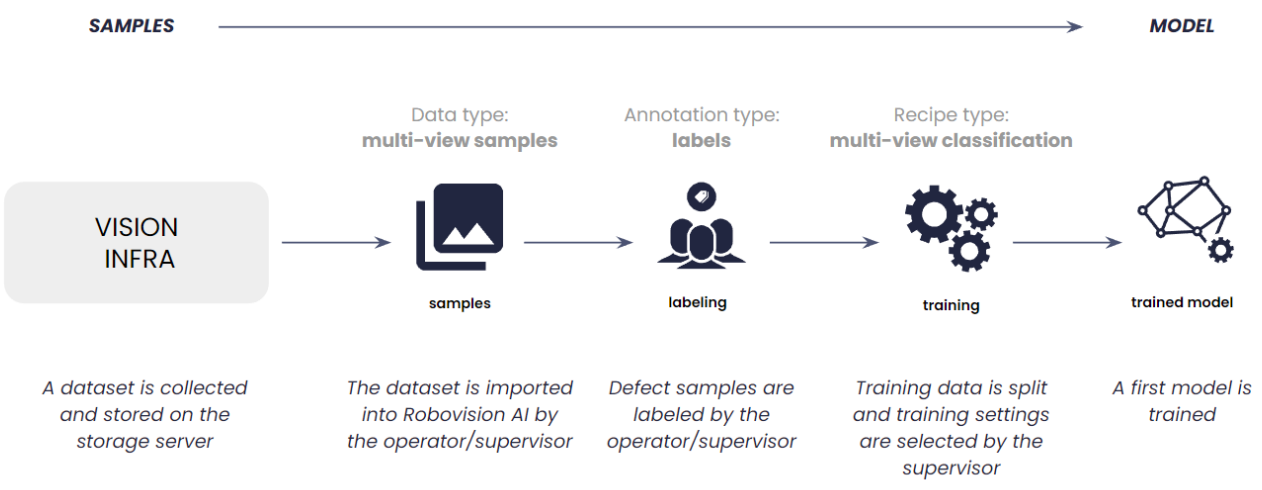
The confidence threshold per class can vary per IC-fabrication layer, depending on actual factory performance. If defects are consistently found in a specific layer of the wafer, for example, the fab operator can modify the recipe to increase the confidence level, allowing for more images to be processed through manual classification. Overall confidence levels can also be tuned in function of available manual classification capacity. The result is a continuous refinement of the model providing higher classification accuracy over a broader range of class types.

Tracking the real "Unknown Ratio" (percentage of classifications that do not reach the confidence level) versus the target "Unknown Ratio" can serve as a trigger for model maintenance or vision infrastructure maintenance.

Minimise Operator Time on Recipe Creation

An ADC solution is no different than any other tool on the manufacturing floor. Just like an etcher or a polisher, ADC executes a recipe and produces a result. Additionally, as with any tool, the tool owner is responsible for creating new recipes and adjusting them from time to time as process changes are implemented.

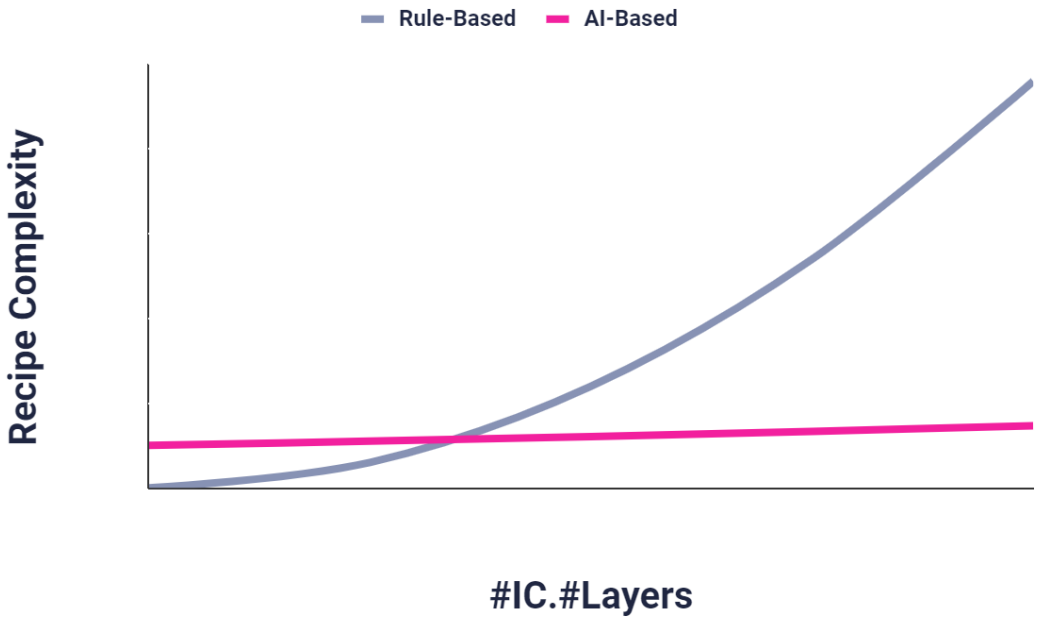
Setting up an ADC is like training your operator. Just as you would subject the human trainee to multiple examples of defects, ADC systems need a similar learning session. Also similar to evaluating a human trainee, it's advisable to assess the learning capabilities of the machine and make minor modifications as necessary, based on the results of the evaluation.



The AI-ADC solution is built with an intuitive UI designed to guide you through the natural steps of collecting/managing samples, configuring image detection, setting up classifiers, and verifying the results. The biggest difference versus training a human however, is that you only need to train a single ADC system, as opposed to a small army of human reviewers.

One size fits all: AI can generalise over different layers and ICs

Defects in the complex chip manufacturing process are specific to the process layer and may depend on the particular IC being fabricated. As such, recipes should either be capable of handling the variation, or they should be customised to the specific layer or specific IC. Rule-based ADC struggles to generalise defects over ICs and process layers due to its nature and consequently requires a consistent customisation effort by highly skilled specialists.



In the process of manufacturing chips, different layers of interconnects in the Back End Of Line (BEOL) can have distinct design rules that result in varying dimensions of defects. However, the characteristics of the defects themselves are comparable across the different layers. Consequently, AI-based recipes can be generalised across multiple layers and multiple ICs, which can significantly increase the efficiency of recipe creation and tuning.

4. Fabrication challenges that AI-ADC can solve

Challenge	Situation	AI ADC Solution
Secure the requisite technical talent	Need for technical talent grows in function of volume	Scale a trained AI model across multiple production lines with minimal operator training
High Frequency of product/IC mix changes	Recipe changes required per IC increase time to production and increase cost	Minimise recipe creation and customisation time
Increasing yield risks due to process variability and contaminations	- Rule based defect classification is unable to detect unknown defect types - Recipe tuning needed for every process update	- Exploit deep learning to detect unknown defects early in the process - Faster HVM after process change

5. Who can use AI-ADC?

The AI-ADC solution can be used in many different cases and industries wherever a machine captures a 2D or 3D signal and where defects can be classified by human inference. Theoretically, if you can train operators to classify your data, then you can reasonably assume that AI-ADC can do the same. On top of that, it can help to identify otherwise overlooked defect types in a timely, consistent and accurate manner.

A single AI-ADC solution can accept results from multiple defect scans and optical review systems in the manufacturing chain, or even across multiple chains. Supported by moderately powered hardware the AI-ADC can process dozens of samples with multi-view images per second, whereas the most skilled humans can only manage around one sample per second.

The high speed, fast data acquisition to handle high volume of high quality training data and reliability allows the AI-ADC to be embedded inline. This means most of the classifications can be done at the same time of, or right after, inspection. This gives engineers the ability to identify problems as early as possible and act accordingly, which translates to better yield and efficiency.

The enterprise-grade AI-ADC solution fits multiple AI maturity levels. For organisations new to deep learning, the AI-ADC allows you to create deep learning models and train/test the model without fiddling with the heterogenous offering of AI libraries. Does your organisation already have models and want to prove it in production? The AI-ADC should allow you to integrate models and fit them into production while enjoying ADC optimised workflows and user experience.